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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,672	07/28/2004	Sheng Wu	13039-US-PA	4671

31561 7590 07/12/2006

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER	
PHAM, THANHHA S	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 07/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

EL

Office Action Summary	Application No.	Applicant(s)	
	10/710,672	WU ET AL.	
	Examiner	Art Unit	
	Thanhha Pham	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) *3 and 18-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-16* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Response to Restriction dated 4/26/22006.

Election/Restrictions

1. Applicant's election of species I in the reply filed on 4/26/2006 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

2. Claims 3 and 18-21 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to nonelected species. ***Notice: *claim 3 that reads on species embodiment II of figures 3A-3F (not species embodiment I of figures 2A-2G) is also withdrawn from consideration.*

Oath/Declaration

3. Oath/Declaration filed on 07/28/2004 has been considered.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

5. Claim 1 is objected to because of informalities. Appropriate corrections are required to clarify scope of claims.

► With respect to claim 1,

line 14, "the underlying first dielectric layer" lacking antecedent basis should be changed to "the first dielectric layer"

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 11-14 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Lin et al [US 6,734,055].**

Lin et al (figs 2's-3's, cols 1-10) discloses the claimed method of fabricating a flash memory, comprising the steps of:

providing a substrate (100, fig 2a);

forming a tunneling dielectric layer (120, fig 2a) over the substrate, wherein the tunneling dielectric layer comprises a silicon oxide layer;

forming a patterned mask layer (130, fig 2a) over the tunneling dielectric layer (120), wherein the patterned mask layer has a trench (140), wherein the patterned mask layer is a silicon oxynitride layer or a silicon nitride layer;

forming a conductive layer (170, fig 2f) over the substrate to cover the surface of the trench;

removing a portion of the conductive layer to form a pair of conductive spacers on the respective sidewalls of the trench to serve as floating gates (175, fig 2g);

removing the patterned mask layer (130, see fig 2k);

forming an inter-gate dielectric layer (180, fig 2i) over the substrate to cover the floating gates (175) and the tunneling dielectric layer wherein the inter-gate dielectric layer is an oxide-nitride-oxide composite layer, an oxide-nitride layer or a silicon oxide layer;

forming a control gate (195, fig 2j) over the inter-gate dielectric layer above the conductive spacers; and

forming source/drain regions (105) in the substrate on each side of the control gate.

7. Claims 1-2, 5-6 and 10 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Kang [US 2004/0119109].

► With respect to claims 1, 5-6 and 10, Kang (figs 2-11, text [0001]-[0048]) discloses the claimed method of fabricating a non-volatile memory, comprising the steps of:

providing a substrate (100, fig 3);

forming a first dielectric layer (tunneling oxide 110, fig 3) over the substrate, wherein the first dielectric layer comprises a silicon oxide layer;

forming a patterning mask layer (115, fig 4) over the first dielectric layer, wherein the patterning mask layer has a trench;

forming a pair of charge storage spacers (140a, storage electrons, fig 6) on the sidewalls of the trench;

removing the patterned mask layer (115, see fig 10 for details);

forming a second dielectric layer (145, fig 7) over the substrate to cover the charge storage spacers and the first dielectric layer, wherein the second dielectric layer is an oxide-nitride-oxide composite layer, an oxide-nitride composite layer or a silicon oxide layer;

forming a conductive layer (150, fig 8) over the second dielectric layer, wherein the conductive layer comprises a doped polysilicon layer;

patterning the conductive layer to form a gate structure (150a, fig 9) over the charge storage spacers;

removing portions of the second dielectric layer (145, figs 8-10) and the first dielectric layer (110, fig 8-10) which are not covered by the gate structure (150a); and

forming source/drain regions (190, 195, fig 10) in the substrate on each side of the gate structure.

► With respect to claims 2, Yang (figs 5-6, text [0032]-[0033]) shows the step of forming the charge storage spacers on the sidewalls of the trench comprises: forming a

charge storage material layer over the substrate; and etching back the charge storage material layer.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kang [US2004/0119109] in view of Liang et al [US 5,714,412].

► With respect to 4, doped polysilicon layer is a known charge storage material for the non-volatile memory. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301. See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960) (selection of a known plastic to make a container of a type made of plastics prior to the invention was held to be obvious). See Liang et al as an evidence that shows using the doped polysilicon layer (18) for the charge storage material. Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Liang et al,

to use the doped polysilicon layer as being claimed for the storage material layer in the method of Kang to provide a function of charge storage in the memory device.

► With respect to claim 7, Kang substantially discloses the claimed method but does not expressly teach forming a dielectric spacer on the sidewalls of the gate structure after patterneding the conductive layer to form the gate structure. However, Liang et al (figs 1-8, cols 1-7) teaches forming the dielectric spacer (28, fig 8) on the sidewalls of the gate structure (20) after patterneding the conductive layer (20) to form the gate structure (see figs 6-8 for details). Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Kang by forming the dielectric spacer as being claimed, per taught by Liang et al to provide a protection to the gate structure in the non-volatile memory.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang [US 2004/0119109] in view of Lin et al [US 6,734,055].

Kang substantially discloses the claim method including forming the patterneded mask layer (115). Kang does not express teach the patterned mask layer is a silicon oxynitride layer or a silicon nitride layer.

However, Lin et al teaches the patterned mask layer can be a silicon nitride layer (130).

Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Lin et al, to use the patterned mask layer with material as being claimed, as known/convenient material, in the process of Kang to provide space for forming the charge storage spacers in the non-volatile memory device.

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kang [US 2004/0119109] in view of Hashimoto [US 2003/0235951].

Kang substantially discloses the claimed method including removing the patterned mask layer but does not expressly teaches performing an wet etching operation using hot phosphoric acid solution to remove the patterned mask layer.

However, Hashimoto shows performing the wet etching operation using hot phosphoric acid solution to remove the patterned mask layer (53) is known and conventional.

Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Hashimoto, to perform the wet etching as being claimed, in the process of Kang to conveniently remove the patterned mask layer for subsequent process steps of forming the non-volatile memory device – since it been known in the art that using the wet etching operation with hot phosphoric acid solution is a convenient technique of cleaning and removing the patterned mask layer with low production cost.

11. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al [US 6,734,055] in view of Liang et al [US 5,714,412].

With respect to 15, doped polysilicon layer is a known material for the conductive layer in forming the floating gates in the flash memory. Selection of a known material based on its suitability for its intended use supported a prima facie obviousness determination in Sinclair & Carroll Co. v. Interchemical Corp., 325 U.S. 327, 65 USPQ 297 (1945) "Reading a list and selecting a known compound to meet known requirements is no more ingenious than selecting the last piece to put in the last

opening in a jig-saw puzzle." 325 U.S. at 335, 65 USPQ at 301. See also In re Leshin, 227 F.2d 197, 125 USPQ 416 (CCPA 1960) (selection of a known plastic to make a container of a type made of plastics prior to the invention was held to be obvious). See Liang et al as an evidence that shows using the doped polysilicon layer (18) for the floating gate. Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Liang et al, to use the doped polysilicon layer as being claimed for the conductive layer of the method of Lin et al to provide a better flash memory with high conductivity of the floating gate.

12. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al [US 6,734,055] in view of Hashimoto [US 2003/0235951].

Lin et al substantially discloses the claimed method including removing the patterned mask layer but does not expressly teaches performing an wet etching operation using hot phosphoric acid solution to remove the patterned mask layer.

However, Hashimoto shows performing the wet etching operation using hot phosphoric acid solution to remove the patterned mask layer (53) is known and conventional.

Therefore, at the time of invention, it would have been obvious for those skilled in the art, in view of Hashimoto, to perform the wet etching as being claimed, in the process of Lin et al to conveniently remove the patterned mask layer for subsequent process steps of forming the non-volatile memory device – since it been known in the art that using the wet etching operation with hot phosphoric acid solution is a convenient technique of cleaning and removing the patterned mask layer with low production cost.

Allowable Subject Matter

13. Claim 17 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TSP

THANHHA S. PHAM
PRIMARY EXAMINER